REMARKS

Claims 1-22 were pending. Claims 1, 6-8, and 16 have been amended and claims 5, 9-12, 14-15, and 17-22 have been canceled. New claims 23-35 have been added.

Claims 1-22 were rejected as anticipated by or unpatentable over KUDO et al. 6,853,037 and claims 1-22 were rejected as unpatentable over KUDO et al. in view of O 7,088,964. Claim 1 has been amended and reconsideration and withdrawal of the rejections are respectfully requested.

Claim 1 has been amended in response to the comments in the Official Action regarding the functional language and to the interpretation of the previously pending claims explained in the Official Action. The amended claims are believed to include structure that distinguishes them from KUDO et al. and O and avoid the shortcomings of the functional language pointed out in the Official Action.

Support for the amendments is found in Figures 3A-C of the present application.

The references do not disclose a device with the MOS transistors and varactor element as defined in the amended claims where the thickness of the second gate insulating film in the varactor element is thinner than the thinnest gate insulating film among the first gate insulating films of the MOS transistors. Accordingly, the amended claims avoid the rejections under §102 and §103.

In the amended claims, the structure of the plural MOS transistors has been further defined so that each has a well with three diffusion regions therein, one of the three diffusion regions being connected to a power source or ground and two others of the three diffusion regions each being connected to a different respective one of a source and a drain, and a first gate insulating film. The amended claims further define the structure of the MOS type varactor element, which has a second conductivity type well with two second conductivity type diffusion regions therein that are connected to a common well terminal (Figure 3C, terminal Vb), a second gate electrode and a second gate insulating film, wherein the gate electrode and the common well terminal have a variable voltage therebetween that corresponds to a variable capacitance between the second gate electrode and the second conductivity type well (page 14, line 27 through page 15, line 3).

Significantly, the varactor element has been structurally defined so that it cannot correspond to a MOS transistor. Note that the two diffusion regions are connected to a common terminal and that the variable voltage between the gate electrode and the common well terminal corresponds to a variable capacitance between the second gate electrode and the second conductivity type well. Accordingly, the interpretation of the previously pending claims is no longer viable.

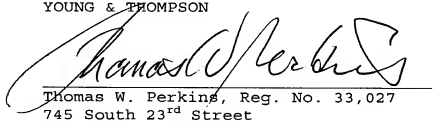
New claim 23 also avoids the applied art. KUDO et al. disclose a semiconductor device with a plurality of MOS transistors having different film thicknesses. O teaches integrating an entire system on a single chip, with CMOS or VCO for varactors in the system. However, O does not teach the claimed relationship between the CMOS gate oxide film thickness and the VCO gate oxide film thickness in a single chip. Accordingly, the new claims are allowable.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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